Proposal: Racing Wheelchair Power Meter

Problem Statement

Paralympic wheelchair racers and coaches need a training system that goes beyond today's heart rate and speed based training regimen. Beneficial coaching information could include power, cadence, direction of pushing force, engagement and disengagement points of the push, data visualization tools, and race replay.

Power measurement is a key performance indicator that has proven to be an effective training tool in sports such as cycling and should be included in any solution.

Current Status

The team currently has a power measurement system that has several limitations:

- Zero point drift –creates distrust and questions of accuracy amongst athletes and coaches
- Integration information on power and heart rate are captured on separate systems, making comparison difficult
- Portability current solution requires a laptop on-board the wheelchair

Proposed Solution

We propose a system solution consisting of bespoke power measurement push rails to monitor power output on both left and right wheels. The push rails communicate over the ANT+ wireless standard with commercially available cyclocomputers and training evaluation software.

The power measurement push rings provide data for power, cadence, and speed. They are extendable to include hand engagement/disengagement points to allow for technique analysis at a later date. The push rails will be transferable between wheels that share identical mounting points. All hardware and electronics will be designed for outdoor use across a full range of temperatures and weather conditions.

Use of the ANT+ wireless standard allows for integration of heart rate with commercially available heart rate monitors. Data collection and on-board display can be through one of many cyclocomputers available through Garmin, CycleOps, Bontrager, and others. All of these solutions weigh only a few hundred grams. Many of them offer additional features such as temperature, road inclination, and GPS, which can be used to further understand training volume and intensity.

Data analysis can also be achieved through commercial or open source software such as Training Peaks or Golden Cheetah, which both accept downloaded data from all ANT+ cyclocomputers. These softwares allow easy data analysis such as time spent in training zones, training stress score, and progress over time.

It may also be possible to interface with real-time trackside monitoring equipment that has already been developed for use in other branches of UK Sport.

The Team (full CVs attached)

This team recently designed and built a similar system for use in a bicycle drag measurement concept. With our combined expertise and recent experience we are uniquely suited to address this problem successfully in the short time frame that is required.

Eric DeGolier

- Bicycle power meter design experience with PowerTap and CycleOps IC trainer products
- MSc dissertation on "Design of a retrofit power-sensing coupling for pumping systems"
- Systems knowledge trained and raced with power for much of the last 10 years including training and racing as part of the U.S. Paralympic team (Athens 2004, tandem pilot)

Dr. Brian Reeder

- M.Sc. Microelectronics Design. B.Sc. Computer & Microprocessor Engineering
- Principal Analogue Electronics Design Engineer
- IC design for power metering products
- Electronic system architecture, detailed schematic designs and PCB layout for a range of measurement products including: ring dynamometers, mains voltage, current and power measurement for commercial metering applications, semiconductor characteristics measurement, frequency measurement, and resistance measurement to 0.1ppm

Rhys Jones

- 20 years design and development experience of embedded systems.
- 10 year experience of Firmware for safety critical applications (very reliable)
- Wireless remote sensor design and development for low power operation.
- Multiple sensor interfacing experience (including strain gauges)

Timeline

Development of the full system will take roughly 8-9 months to complete on a parttime basis. This could be shortened to 5-6 months if the existing measurement system (hardware) can be used, as then a majority of the work is in the analogue and digital electronics.

Please contact Eric DeGolier: Mobile – 07872 180 250 Email – eric@vortexsportdesign.com

Eric DeGolier (MSc, BSME)

25 The Avenue, Flat 3 London W13 8JR **Phone:** 0787 218 0250

E-mail: eric@vortexsportdesign.com Nationality: United States of America

I am an experienced design engineer with a strong background in creative design and team leadership. With a background in elite athletics I gravitate towards, and excel at, challenging sporting projects

Employment

2009-now

Managing Director, Vortex Sport Design, London

- Designed and prototyped patent pending aerodynamic drag measurement system

- Coordinated team of electrical and mechanical engineers to complete project

- Responsible for all project management, timelines, vendor relations

Senior Design Engineer, DeepStream Technologies, Bangor Wales

- Created projects for intelligent energy management

- Led teams of engineers on concept and development projects

2005-2006

Design Engineer, Trek Bicycles, Waterloo, WI, USA

- Designed products for high precision, automated manufacture

- Designed bicycle accessories in multi-disciplinary teams
- Created cycling products in a range of plastics, steel, aluminium materials
- Designed for manufacture with injection moulding, forging, casting, extrusion, bending, stamping, welding
- Worked directly with suppliers in Taiwan and China

2002-2005

Design Engineer/Test Engineer, Saris Cycling Group, Madison, WI, USA

- Apprenticed under product designer Fabio Pedrini for 6 months in Italy
- Worked with elite coaches to develop suite of training systems for indoor bike trainer
- Adapted power measuring system for fixed gear bicycles and trainers
- Organized test standards and testing lab for the company
- Designed individual tests working with accelerometers, strain gauges, temperature sensors, dB metres, and various other instruments
- Designed and tested high RPM bike trainers for balance and fatigue

2000

Work experience, LasX Industries, White Bear Lake, MN, USA

- Designed specialised conveying system for laser cutting operation
- Automated sheet-based laser-cutting operations

Computer Skills

Multiple CAE softwares

- SolidWorks 3D modeling-6 yrs
- Cosmos FEA-2 yrs
- ANSYS FEA-1.5 yrs
- Pro E 3D modeling-1 yr

Other softwares

- Microsoft Office programs
- Programming in C++, Java, machine language

Good familiarity with:

- Matlab
- -Simulink
- Labview
- -P-Spice
- Mplab
- -ADAMS

Education

2006-2007

Design Engineering MSc, Brunel University, College of Engineering and Design (Distinction, Alumni Award for Best Dissertation)

- **Dissertation project** 'Design of a retro-fit power sensing coupling for pumping systems using triple-beam tuning fork strain gauges.'
- Design project Mobile elevated work platform, designed from initial requirements through final drawing package, including FEA, static and dynamic analysis of system
- **Modules studied** include: structural design and FEA, design of mechatronic systems, advanced computer aided engineering, microcontrollers and digital control, human factors in design
- **Software learnt**: ADAMs, Matlab, Simulink, Pro Engineer, SolidWorks, Cosmos, ANSYS, P-Spice, Mplab, VPic
- **Additional courses** outside of classwork taken: Successful Teamworking, Life Drawing, Effective Networking

1998-2001

Bachelor of Science in Mechanical Engineering, University of Wisconsin–Madison, College of Engineering Overall GPA: 3.0 Mechanical Engineering GPA: 3.12 (out of 4.0)

- Relevant experience: Future truck aerodynamics team (wind tunnel testing and CFD analysis)
- **Software learnt**: Pro Engineer, SolidWorks, ANSYS, Fluent, Labview, Matlab, MAPLE
- **Instrumentation used**: analogue and digital oscilloscopes, dynamometer, wind tunnel, spectrum analyser, infrared temperature sensor, thermocouple

Skills and Achievements

2006, 2009	Inquisitive – '06 Taught myself carbon fiber lay-up techniques and made several prototypes, '09 Taught myself thermoset moulding techniques to create elastomer prototypes
2004-2005	Versed in design - studied for 6 months under an experienced product designer
2004-2005	Well spoken - Speaking engagements, from 5-100 people, talking about my Paralympic experience, Alumni Prize for Best Disertation – Brunel University
2004	Focused - Member of U.S. Paralympic Team, Athens, Greece
2002	Self motivated - Contested Innovation Day invention competition as an undergraduate http://www.engr.wisc.edu/news/exhibits/StudentInnovation/7.html
2001	Team player - Member UW Future Truck Team, 2 nd place, high mileage vehicle contest
2001	Able to multi-task - "All American Team" Collegiate National Cycling Championships while maintaining 3.0/4 average in school

Interests

Cycling, camping, Nordic skiing, adventure travel Composite materials, consumer electronics

Dr. BRIAN MARTIN REEDER

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SUMMARY

Analogue / Mixed Signal Principal Design Engineer with good attention to detail and a recognized ability to generate novel solutions. Values the opportunity to work in a challenging environment involving analogue circuit design and layout. Possesses D.Phil. and M.Sc. in Microelectronic System Design. Recent experience in:

- CMOS Technology
- Cadence Design Software
- Spice, Pspice & Switcap2 Simulators
- Matlab & Mathcad

- Mixed Signal Design
- Altium Dxp Design Software
- Embedded C & Labwindows CVI
- Solidworks

EMPLOYMENT HISTORY

Contract Design - Bangor, Gwynedd

2009 - Now

Hardware design, PCB layout, assembly and test for several start-up companies with projects including:

- Mains power metering and control systems
- Managed Ethernet switch and Wi-Fi interfaces,
- Dynamometer with force & moment measurements system
- Off-Line SMPS design

DeepStream Technologies - Bangor, Gwynedd

2004 - 2009

Analogue / Mixed Signal Design

- Principal Design Engineer (2006 2009)
- (2004 2006)- Senior Design Engineer

Specification, definition and design of mixed signal circuits for a variety of mains measurement system modules. Tasks undertaken include:

- Design of system architecture in compliance with customer requirements,
- Definition of mixed signal ASIC architecture and requirement specifications,
- Liaison with ASIC designers and manufacturers throughout design cycle,
- Evaluation of completed ASIC and verification of performance in accordance with specification,
- System & ASIC performance analysis using Matlab, Mathcad and Excel,
- Design and specification of all other system circuit elements including PSU and micro-controller,
- Design of embedded software algorithms for system hardware control and measurements,
- Schematic capture, simulation and PCB design using Altium Dxp,
- Manufacture of PCB prototypes using CircuitCam, BoardMaster and an LPKF router system,
- Preparation of patent applications for novel system aspects.

Contract Design - Austin, Texas

2002 - 2003

PC based test system hardware design, construction and software generation using Labwindows CVI to implement the following elements:

- 24 bit delta sigma ADC control,
- Synchronous control of multiple ADC's for DMM application,
- Synchronous control of multiple DAC's,
- Integration of ADC and DAC's for semiconductor characteristic plotter,
- 100MHz counter/timer with seven digit display,
- Thermal probe and ambient temperature measurement.
- Ambient humidity measurement,
- Low ohmic value resistance measurement,
- Ni-Cad battery charger and eprom programmer.

Cirrus Logic - Austin, Texas

Analog / Mixed Signal IC Design - Senior Design Engineer

Specified, defined and designed mixed signal CMOS integrated circuits using Cadence including:

- Switched capacitor amplifier and DC level shifter of an A to D converter front end for use in motor fault prediction by acoustic monitoring,
- High-voltage, single-transformer, isolated power, clock and bi-directional data transfer system for power measurement applications. Included amplifiers, fast comparators, synchronous rectifier and custom pad driver components.

MEM Low Voltage Devices (<250v) - Holyhead, Anglesey, Wales.

1997 - 2000

Mixed Signal ASIC Design - Senior Design Engineer

Specified and defined mixed signal CMOS integrated circuits for a digital residual current circuit breaker application in collaboration with Cirrus Logic. This included high voltage isolation and protection, current sensors, analogue front end, A to D converters and data processing elements.

- Performed theoretical system error analysis and produced system simulator using Matlab.
- Developed and built 0.1ppm measurement system for component performance verification.
- Designed prototype system hardware with appropriate software control using Labwindows.
- Schematic capture, simulation, PCB design and construction of element prototypes using Altium Dxp.

Marconi Instruments Automation Division – St. Albans, Hertfordshire, England. 1982 - 1991 Projects Manager, 1987 - 1991

Coordinated with Product Managers to identify customer requirements and new product ideas. Controlled investigation, definition and development of in-circuit test systems. Planned and controlled automatic test equipment projects. Prepared project and department budgets. Managed product support, technical publications, PCB design and mechanical design departments and engineering technicians.

Test Engineering Manager, 1985 - 1987

Included responsibilities indicated below and managed technical publications department that generated system installation, operation and service manuals. Attended GEC's test and measurement special interest group to co-ordinate test procedures and equipment throughout all GEC companies.

Senior Engineer/Section Leader, Test Engineering, 1984 - 1985

Prepared department budgets, planned and allocated work of six engineers/technicians. Resolved production and service measurement problems. Specified requirements and procurement of production test equipment.

Graduate Engineer, Test Engineering, 1982 - 1984

Designed automatic in circuit test system tests, including goods inward test procedures for components and production test procedures for sub-assemblies and systems. Designed and manufactured test and calibration equipment.

EDUCATION

University of Sussex - Falmer, East Sussex, England.

1993 - 1997

D.Phil., Space Science Centre

Researched application of artificial neural networks for satellite instrument data compression.

- Obtained appropriate satellite data and manipulated it for suitable data compression evaluation.
- Created artificial neural network simulator running on PC.
- Designed neural network architecture for data compression and evaluated compression performance.
- Adequate data transmission simulation results were obtained with compression ratios up to 40:1, representing a four-fold improvement over existing techniques.
- Published Application of Artificial Neural Networks for Spacecraft Instrument Data Compression,
 Brian M. Reeder & M. Paul Gough, Microprocessors and Microsystems (20) 1996 pp285-295.

Supervised undergraduate laboratories: semi & full custom IC design using Chipwise, gate array design, PAL design, computer aided design (schematic capture, simulation and layout), analogue electronics, microprocessor systems including Z80 Assembler, Modula 2 programming, logic system design and Microsoft's Word and Excel.

M.Sc., Microelectronic System Design

Course included: Analogue Design, Chip Architecture, Signal Processing, VLSI Arithmetic, Fabrication Technology, Advanced Logic Synthesis, Sequential and Parallel Computer Architecture, Software Engineering and Computer Aided Design.

- Semi-custom CMOS design assignment of adaptive digital filter for hearing aid acoustic feedback cancellation. Resulted in fabrication of the designed IC.
- Full-custom CMOS design assignment for content addressable memory. Resulted in fabrication of the designed IC.
- Mixed analogue/digital project to design artificial neural network IC. It included 256 D to A converters, 1024 switched capacitor resistors connected in an eight-dimension, hyper-cubic network and an A to D converter. Resulted in completed design, but insufficient funds were available for fabrication.

University of Essex - Colchester, Essex, England.

1978 - 1981

B.Sc. Computer & Microprocessor Engineering, Class 2,2.

- Undertook vacation project at British Telecommunications, Martlesham Heath Research Station.
 Project was for quantitative measurement of integrated circuit internal waveforms using electron beam microscope probe.
- Carried out vacation project writing software package for British Telecommunications, Blackburn telephone area accounts department. Software summarized engineering manpower expenditure for management reports.

Curriculum Vitae

Rhys Jones

Date Of Birth: 14th March, 1968. Nationality: British.

Marital Status: Single. Children: None.

Address: Pen Rhos, Rhosfawr, Pwllheli, Gwynedd, LL53 6UU.

Telephone - Home: (01766) 810476 mobile: 07824 811484

e-mail - Home: rhysj yah@yahoo.co.uk

e-mail - Work: service@embedded-magic.co.uk

Experience Overview

- Design experience with ARM7, AVR (Mega), PIC, TMP90C640, 6805, 8031, 8088
- Over 10 years of firmware design experience mostly for safety critical applications
- 20 years total design and development of hardware & embedded software
- Design and development of various high-speed and complex digital circuits with discreet logic, CPLD and FPGA design utilising both 'Altera' & 'Xilinx' environment.
- Analogue instrumentation design for measurement and control.
- Data conversion and digital filtering to obtain greater accuracy and resolution than provided by ADC.
- Electro-mechanical product design: robotics, RCD, industrial equipment.
- Familiar with the architecture of the IBM PC and its operation having designed ISA & PCI bus slot-in cards (for data acquisition and control), security dongles with accompanying software. Written MS-DOS and Windows Device Drivers, TSRs and application software with a Graphical User Interface for Windows XP, Vista & 7.
- Busses, protocols and hardware interfaces: STE bus (IEEE1000), PCI, ISA, IEEE 802.3, CAN, HDLC, RS485, RS232, USB, GPIB, SPI, I²C along with various customised serial protocols. Developed custom hardware and protocol stack.
- Wireless development with Bluetooth, ZigBee, and telemetry using GSM and Iridium.
- Experience of providing documentation covering the design and development of software, hardware and mechanical drawings to meet BSI/ISO standards.
- Experience of 'CE' and 'UL' certification and "hands-on" EMC testing.
- Products support for both customer/end user and assembly line.

Employment History

January 20010 to Present: Trading as "Embedded Magic"

URL: www.embedded-magic.co.uk

Design and development of digital USB camera for medical applications using custom sensor and motors for extended view.

Development of system for monitoring temperature, thickness and position of sea ice. This involved interfacing with GPS unit and transmitting data via Iridium satellite modem. Very low power consumption requirement for operation on battery pack in remote location for many years. Module is reconfigurable via Satellite modem.

Design and development of low power Zigbee (wireless) based remote sensor. The design required multiple digital signal conditioning techniques for very precise measurement in harsh environment.

March 2004 to May 2009: DeepStream technologies Ltd

Position: Senior Design Engineer

Firmware design for a safety critical product (C and assembler). Great emphasis on code efficiency for both code size and processing overhead for minimal power consumption. Maximum accuracy and resolution obtained from multiple sensors inputs using novel data acquisition techniques. Developed flexible feature set for customer products. Feature set may be programmed at the factory or (wirelessly) configured and re-calibrated later in the field. Other duties include hardware design and development, aiding and supervising IEC standard testing of product, hardware definition and trouble shooting, ATE cell development.

May 2003 to March 2004: Freelance design engineer

- 1. Network existing hand held air quality meters. System uses off-the-shelf CAN bus technology as the transport layer, custom network and application layer developed allows the system to dynamically configure itself. Sole responsible for the concept and design of the network hardware, firmware, and network protocol.
- 2. Development of a Windows based GUI for robotic measurement apparatus.
- 3. Creation of automated, PC controlled, environmental test chamber for multi-cycle freezing of aggregate along a defined curve. Maintenance of industrial test equipment and modification of existing test apparatus.

April 2001 to May 2003: Delta Electrical Ltd., Holyhead, Anglesey

Position: Senior Design Engineer

Heading a team of 4 people having performed research and leading development of novel multi-drop communication system for switchgear. Produced communication device prototype with the following properties: electrically isolated bus, inbuilt message priority system, simple analogue components. The design utilises 2 different modulation techniques to achieve both prioritised channel arbitration and fast message transfer.

October 1999 to April 2001: Sharp (UK) Ltd., Wrexham, Flintshire

Position: Senior Design Engineer (Hardware)

Part of a 6-man team involvement in the development and test of Ethernet (802.3) module for a colour FAX machine. Sole responsible for the hardware design in for the conversion of a industrial FAX machine to being Ethernet enables. The add-on module is based on an ARM7 core with an integrated MAC unit, using FPGA and Dual-Port memory to interface to the FAX itself. Following the successful handover of the project I spent 6 months investigating the operation of a GSM mobile phone along with the associated hardware, software and support. Test procedure and performance criteria were also analysed for pre FTA compliance checking.

May 1994 to October 1999: EURO/DPC Ltd., Llanberis, Gwynedd

Position: Electronic Design Engineer

Working in a small team of engineers involved in the design of laboratory equipment automation. Products include 3 linear axis system, stepper motors driven with feedback sensors for accurate positioning and speed control where real-time analysis of movement is necessary; stand alone PIC & 8031 based products. Separate PCI cards design with the associated Windows NT driver (using NT 4.0 DDK) for external customer. Duties include all aspects of hardware and embedded software design, in assembler and 'C', through to EMC testing and manufacturing. Documentation of product design to meet 'CE', 'UL' and ISO9000.

September 1992 to May 1994: A.D.E. Ltd., Liverpool.

Position: Software Engineer

Responsible for the design and development of software for a 30 zone alarm control panel and aiding the continuing development of a new serial, multi-zone monitoring system. Real time, multi-tasking software is used within an embedded Toshiba 8 bit microcontroller. Reliability and robustness was a major software design consideration. User control is via 4 remote LCD keypads incorporating 6805 and 8051 microcontrollers.

September 1989 to August 1992: GEC-Plessey Avionics, Portsmouth.

Position: Engineer

Designed and developed a complex R.F. control unit as part of a comprehensive test equipment for a radar based missile detector. The unit, based on an embedded 8031

microcontroller, operated as a slave controlled via PC driven menu system. The internal functionality included variable, accurate digital I and Q frequency synthesis designed into a FPLD as well as various other complex sequencing and control operations.

Part of a team involved in the design and development of a 2nd generation, modular Missile Approach Warner system for aircraft. The apparatus performed signal conditioning (baseband conversion), data acquisition and analysis. Manipulation and transformation of accumulated data was performed using DSP methods with various inter-module and external data transfer methods being employed. The prototype unit incorporated four TMS320C40 processor cards in addition to a dedicated FFT processor.

Higher Education

1986-1989 University College of North Wales, Bangor, Gwynedd. Degree: Electronic & Electrical Engineering, BSc Honours.

Experience Summary

Programming Languages and Assembler:

High Level: 'C', Pascal, FORTRAN, BASIC & Visual Basic, HTML

Assembler: PIC, 80x86, 8031, 6805, TMP90C640, TMS320C10/25, ARM7, AVR Compilers: VB6, Visual Studio (2002, 2005, 2008), IAR, Hi-Tech, Keil, MCC18, C30

Operating Systems:

MS DOS (Ver 3.2 to 6.22), WINDOWS 3.x, 95/98, NT (4.0 & 2000), XP & Vista, Windows 7

CAD/CAF

PADS, Seetrax, OrCAD, EasyPC, Futurenet, Altium (Protel), ABEL, FPGA, CPLD & PAL design tools, Teamwork, PSPICE, AutoCAD, Mechanical Desktop, SolidWorks

Training Courses:

Real Time, Structured Analysis Structured Design Course (Yourdon Methodology)

Plessey Graduate Management Training Scheme

Various team leadership and management training programs

Advanced PLD and FPGA

Advanced AutoCAD

ARM7 - foundation course

PRINCE2 – Project Management. (Foundation and practitioner)

Interests, Skills and Leisure Activities:

Photography and mountain walking I find to be a rewarding complementary pastime

Sports: Rock climbing, cycling, running

Achievements: 300mile (3 day) sponsored cycle ride. London marathon in 1997 and 1999

Fluent in the Welsh Language

Full car and motorcycle driving licence